UD info
宇達資訊

Toshiba NAND Flash Reliability Note

Date: Nov. 21, 2016

15nm MLC NAND Flash Reliability Note

Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

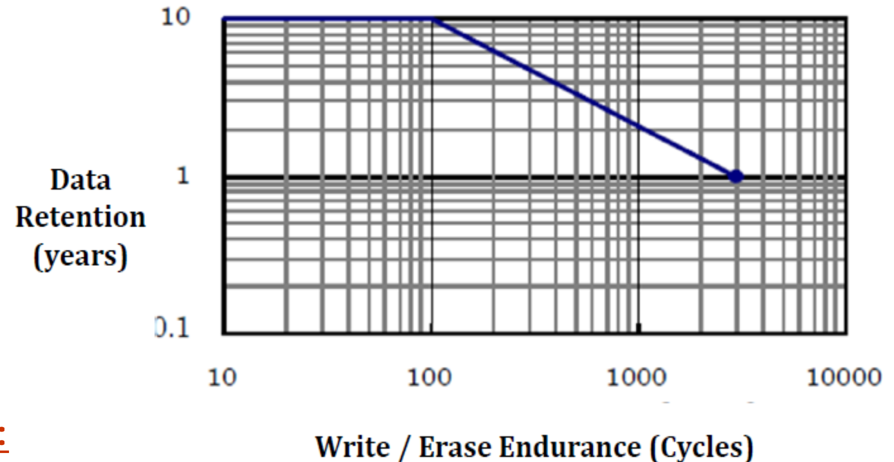
	Write/Erase Cycles (Cycles)	Cumulative Block Failure Rate
MLC	3,000	Less than 0.04

Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

Here are the combined characteristics of Write/Erase Endurance and Data Retention.

Write/Erase Cycles (Cycles)	Estimated Data Retention (Years)
Initial (Less than 100)	10
3,000	1



Condition of Data Retention Estimate:

- Vcc=3.3V, Ta=40 ℃, ECC=40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Toshiba 15nm MLC

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15nm Pseudo SLC (pSLC) Reliability Note

Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

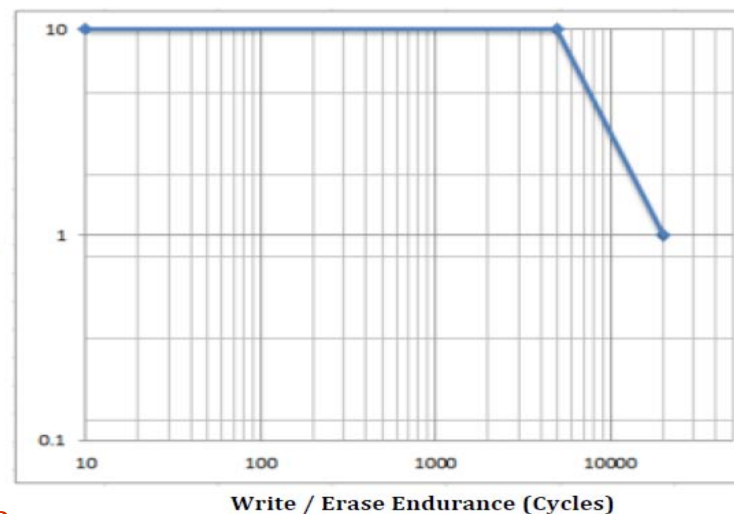
	Write/Erase Cycles (Cycles)	Cumulative Block Failure Rate
pSLC	30,000	Less than 0.04

Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

Here are the combined characteristics of Write/Erase Endurance and Data Retention.

Write/Erase Cycles (Cycles)	Estimated Data Retention (Years)
Initial (Less than 100)	10
30,000	1



Condition of Data Retention Estimate:

- Vcc=3.3V, Ta=40 ℃, ECC=40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Toshiba 15nm pSLC

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24nm SLC NAND Flash Reliability Note

Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

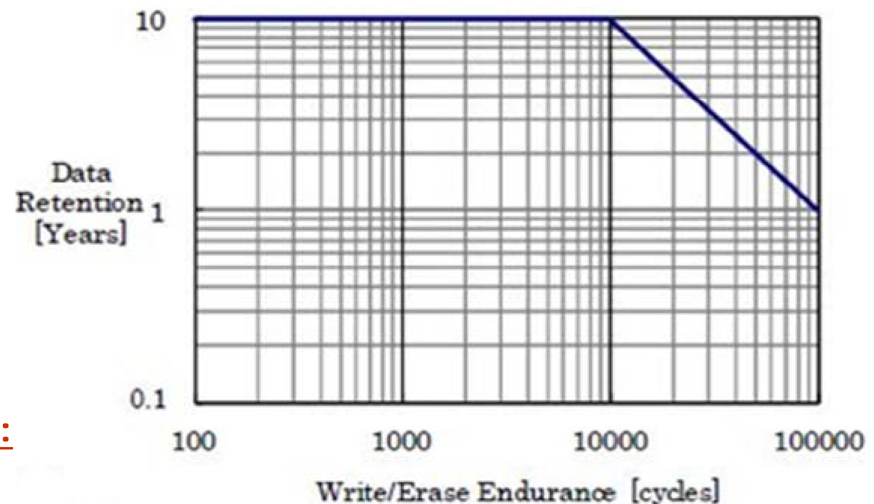
	Write/Erase Cycles (Cycles)	Cumulative Block Failure Rate
SLC	100,000	Less than 0.04

Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erase and reprogramming, the block may become usable again.

Here are the combined characteristics of Write/Erase Endurance and Data Retention.

Write/Erase Cycles (Cycles)	Estimated Data Retention (Years)
Initial (Less than 100)	10
30,000	3
100,000	1



Condition of Data Retention Estimate:

- Vcc=3.3V, Ta=40 ℃, ECC=40bit/1KB
- All Pages in blocks are tested with Random data
- DUT = Toshiba 24nm SLC

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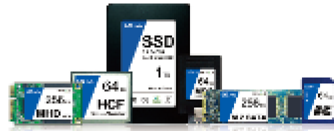

Thank you